

<b>Notice of References Cited</b>	Application/Control No. 09/941,952	Applicant(s)/Patent Under Reexamination WHEELER ET AL.	
	Examiner Russell Frejd	Art Unit 2128	Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-2003/0046649	03-2003	Wheeler et al.	716/12
	B	US-2003/0046648	03-2003	Wheeler et al.	716/11
	C	US-2003/0046642	03-2003	Wheeler et al.	716/2
	D	US-2003/0046640	03-2003	Wheeler et al.	716/1
	E	US-2003/0046054	03-2003	Wheeler et al.	703/15
	F	US-2003/0046053	03-2003	Wheeler et al.	703/15
	G	US-2003/0046051	03-2003	Wheeler et al.	703/14
	H	US-6,721,925	04-2004	Wheeler et al.	716/2
	I	US-6,708,321	03-2004	Wheeler et al.	716/18
	J	US-6,643,836	11-2003	Wheeler et al.	716/11
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	JEFFERY et al., M. Monte Carlo Optimization of Superconducting Complementary Output Switching Logic Circuits, IEEE Transactions on Applied Superconductivity, Vol. 6, No. 3, September 1998, pages 104-19.
	V	MITRA et al., S. Design Diversity for Concurrent error Detection in Sequential Logic Circuits, 19th IEEE Proceedings on VLSI Test Symposium, May 2001, pages 178-83.
	W	
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.